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10/723,530	11/24/2003	David Lewis	174/304	8666

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EXAMINER	
TRAN, ANH Q	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 09/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/723,530	LEWIS, DAVID	
	Examiner	Art Unit	
	Anh Q. Tran	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,8-11 and 13-37* is/are rejected.

7)☒ Claim(s) *4-7, 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 13 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claim recites "wherein the second stage has first, second, third, and fourth combination signal outputs" is vague and indefinite since figures 1-3 show that first and second stages produced first, second, third, and fourth combination signal outputs. Furthermore, which figures show the XOR produce two further signals? Clarification is required.

3. claims 14-15 are rejected as dependent on claim 13.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-3, 8-11, 16-20, 25-31, 32-37 are rejected under 35 U.S.C. 102(b) as being anticipated by Swami (2002/0116426).

Swam shows:

1. Logic module circuitry (Fig. 3) comprising:

combinational logic circuitry having at least first (13a, 13b), second (13d, 13c), and third stages (28/32A), each of said stages being responsive to at least one input of the logic module (13a and 13 response to A & B, and third stages, 28/32A, response to D); and XOR circuitry (17-1A and 15-1A, output of 15-1A, CYO, connected to an input of 26-2A) interposed between two of the stages or between the third stage and an output of the combinational logic circuitry for logically combining a carry in signal (Cyin) with at least one combinational signal (C_L and C_Li) in the combinational logic circuitry.

2. The circuitry defined in claim 1 further comprising:

programmably controlled circuitry (13-2A) for selectively disabling the carry in signal.

3. The circuitry defined in claim 1 further comprising:

circuitry (17-2A, 22A, and 15-2A) for producing a carry out signal (Cyout) from the carry in signal (CYO) and combinational signals (C_UC and C_Ui) in the combinational logic circuitry.

8. The circuitry defined in claim 1 wherein the combinational logic circuitry has first (11-1A, 11-2A, 11-3A, 11-4A), second (13a, 13b), third (13c, 13d), and fourth stages (28/32A), and wherein the XOR circuitry is interposed between the third and fourth stages.

9. The circuitry defined in claim 1 wherein the XOR circuitry (XOR input C_Li is output from 13b which is the second stage and CYO is connected to 26-2A which between 13b and 28/32A) is interposed between the second and third stages.

10. The circuitry defined in claim 1 wherein the third stage [(here first stage are 11-1A, 11-2A, 11-3A, 11-4A), second stage are (13c, 13d), third stage are (13a, 13b), and fourth stages (28/32A)] has first (C_L) and second combinational signal outputs (C_Li), and wherein the XOR circuitry (17-1A) logically combines the first combinational signal output with the carry in signal (Cin) to produce a sum out signal (CYO).

11. The circuitry defined in claim 10 further comprising:

circuitry (17-2A, 22A, 15-2A) for producing a carry out signal (Cyout) from the carry in signal and the first and second combinational signal outputs (CYO is carry in signal and the first and second combinational signal outputs).

16-18. the first and second stages are programmable to produce an output signal that is usable in forming an arithmetic sum, difference, and product of first and second stage input signals.

19. The circuitry defined in claim 18 wherein the third stage and the XOR circuitry are operable to form the arithmetic sum of the output signal, a third stage input signal (D), and a carry in signal (Cyin).

20. A programmable logic device logic module circuitry as defined in comprising claim 1.

25-31. the apparatus described above is applicable to the method claims.

32. Logic module circuitry (Fig. 3) comprising:

look-up table circuitry having first (11-1A, 11-2A, 11-3A, 11-4A), second (13a, 13b or 13c, 13d), third (13c, 13d or 13a, 13b), and fourth stages (28/32A); and XOR

circuitry (17-1A, 15-1A) logically combining a carry in signal (Cin) with signal information from a source stage (13a, 13b) to produce further signal information applied to a destination stage (28/32A), wherein the source stage is selected from the group consisting of the second and third stages, and wherein the destination stage is the third stage if the source stage is the second stage, and the destination stage is the fourth stage (28/32A is destination stage) if the source stage is the third stage (13a, 13b).

33. The circuitry defined in claim 32 further comprising: circuitry (13-2A) for selectively disabling the carry in signal.

34. The circuitry defined in claim 32 further comprising: circuitry (17-2A, 22A, 15-2A) for producing a carry out signal (Cyout) from at least the carry in signal and signal information from the source stage (CYO is combination signals of C_L; C_Li, and Cin).

35. The circuitry defined in claim 34 wherein the circuitry for producing is connected so that the carry out signal is based in part on a third stage input signal (A, B).

36-37. The circuitry defined in claim 32 wherein the look-up table circuit leading to the XOR circuitry includes circuit elements that are programmable so that the signal information from the source stage that the XOR circuitry receives is indicative of a result of arithmetically adding or multiplying together first and second stage input signals (ANDing and ADDing A, B, Ci, Di are by 14-1A to 14-16A, Fig. 2).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 21-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Swami (2002/0116426) in view of Park et al (6,359,468).

Swami discloses the claimed invention except for a memory, processing circuitry, and programmable logic device mounted on a printed circuit board. Park discloses a memory, processing circuitry, and programmable logic device mounted on a printed circuit board. It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the programmable logic device of Young in a digital processing system of Park, in order to provide wide variety of applications where the advantage of using programmable logic device.

Allowable Subject Matter

5. Claims 4-7, 12, 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh Q. Tran whose telephone number is 571-272-1813. The examiner can normally be reached on M-TH (7:00-5:30) Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on 571-272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANH Q. TRAN
PRIMARY EXAMINER

9/12/05